Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.257”**

**.257”**

**SOURCE**

**GATE**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: S = .052” X .069” G = .018” X .028”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .257” X .257” DATE: 7/11/22**

**MFG: IR THICKNESS .015” P/N: IRFC150**

**DG 10.1.2**

#### Rev B, 7/19/02